REMARKS

Claims 9-16 are now pending in the above-referenced application.

Claims 9-11 and 13-16 stand rejected under 35 U.S.C. 35 U.S.C. § 103(a) as being unpatentable over Mergard.

The claimed invention shows a serial shift register which is controlled by the timer outputs to transmit the data and to realize the parallel to serial conversion. In Mergard the processor itself writes into a register which means that this function results in a load for the processor. On the contrary, the claims as amended recite that the recited data transmitting occurs without loading the CPU. Support for this amendment is found at least in page 3, lines 25-31, of the specification. In the claimed invention, the writing into the shift register is done by hardware, not by the CPU itself. So in the claimed invention there is a shift register with the pin-states and no CPU activity, and no load for the CPU is necessary. Mergard only describes an SPI interface, which means the necessity of address and control signals, in other words, a CPU load. These address and control signals are not necessary in the claimed invention because the recited shift register is controlled by the timer outputs with a given frequency to transmit the data without needing CPU activity and without address and control signals. Thus, the claimed invention describes a very simple method to transmit data between a microcontroller and an output stage independent from address and control signals and independent from CPU activity. As a consequence, the CPU is not burdened by controlling the transmission and is not loaded by that controlling operation.

Accordingly, Applicants request that the rejections be withdrawn, and that the present application issue as early as possible.

Respectfully submitted,

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Dated: 8/23/06

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